What is claimed is:

1. A method for fabricating a multi-bit vertical memory cell, comprising:

providing a semiconductor substrate having a trench;

forming doped areas, acting as bit lines, in the semiconductor substrate near its surface and the bottom of the trench;

forming bit line insulating layers over each of the doping areas;

forming a conformable oxide layer over a sidewall of the trench and the bit line insulating layers to locally store electric charge; and

forming a conducting layer over the insulating layer and filling in the trench.

2. The method for fabricating a multi-bit vertical memory cell of claim 1, a fabricating method of the doping areas further comprising:

forming a spacer over the sidewall of the trench; and

performing ion implantation in the substrate using the spacer as a mask; and

removing the spacer.

3. The method for fabricating a multi-bit vertical memory cell of claim 2, wherein the spacer is silicon nitride.

4. The method for fabricating a multi-bit vertical memory cell of claim 2, wherein phosphorous ions are implanted.

5. The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the bit line insulating layers are formed by thermal oxidation.

6. The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the thicknesses of the bit line insulating layers are 300 to 2000Å.

7. The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the oxide layer is a silicon rich oxide layer.

8. The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the thickness of the oxide layer is 50 to 110Å.

9. The method for fabricating a multi-bit vertical memory cell of claim 1, further comprising a gate dielectric layer between the oxide layer and the trench surface.

10. The method for fabricating a multi-bit vertical memory cell of claim 9, wherein the gate dielectric layer is a gate oxide layer.

11. The method for fabricating a multi-bit vertical memory cell of claim 9, wherein the thickness of the gate dielectric layer is 50Å.

12. The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the conducting layer is a poly layer.

13. A multi-bit vertical memory cell, comprising:

a semiconductor substrate having a trench;

bit lines formed in the substrate near its surface and the bottom of the trench;

bit line insulating layers disposed over each of the bit lines;

a silicon rich oxide layer conformably formed over a sidewall of the trench and the bit line insulating layers to locally store electric charge; and

a word line disposed over the silicon rich oxide layer and filled in the trench.

14. The multi-bit vertical memory cell of claim 13, wherein the bit lines are formed by phosphorus ion implantation.

15. The multi-bit vertical memory cell of claim 13, wherein the thicknesses of the bit line insulating layers are 300 to 2000Å.

16. The multi-bit vertical memory cell of claim 13, wherein the bit line insulating layers are oxide layers.

17. The multi-bit vertical memory cell of claim 13, wherein the thickness of the oxide layer is 50 to 110Å.

18. The multi-bit vertical memory cell of claim 13, further comprising a gate dielectric layer between the silicon rich oxide layer and the trench surface.

19. The multi-bit vertical memory cell of claim 18, wherein the thickness of the gate dielectric layer is 50Å.

20. The multi-bit vertical memory cell of claim 13, wherein the word line is a poly layer.